1.1 Logic gates :

Logic gates are the devices used as basic building blocks of all digital circuits. By connecting the gates we can build circuitry that can perform arithmatic.

* Classification of Logic Gates :

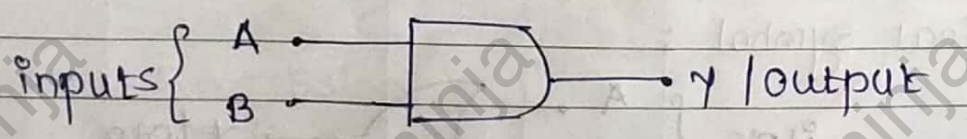
Logic Gates

- Basic Gates
  - ① AND gate
  - ② OR gate
  - ③ NOT gate
- Universal Gates
  - ① NAND gate
  - ② NOR gate
- Special purpose Gates
  - ① Ex-OR gate
  - ② Ex-NOR gate

1) AND Gate :

Def^n - It performs logical multiplication operation. The o/p of AND gate is high if and only if all the inputs to the gate are high.

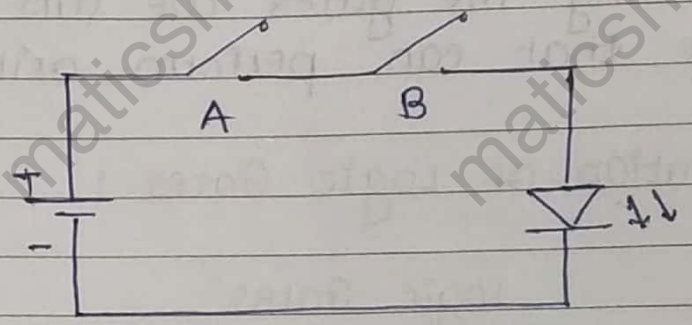
Symbol :



Boolean Expression :

$$Y = A \cdot B$$

Switching Circuit :



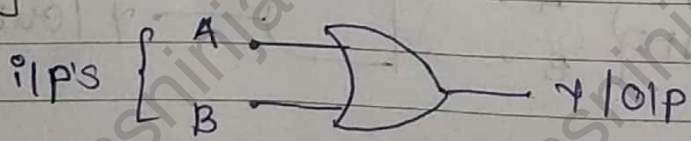
Truth Table :

Inputs		Output
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

2] OR gate :

Defn : It performs logical addition operation. The o/p of OR gate will be high if any are or both the inputs are high.

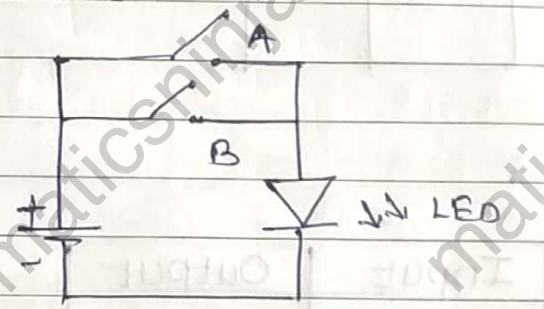
Logical Symbol :



Boolean Expression :

$$Y = A + B$$

Switching Circuit :



Truth Table :

Inputs		Output
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

3] NOT Gate :

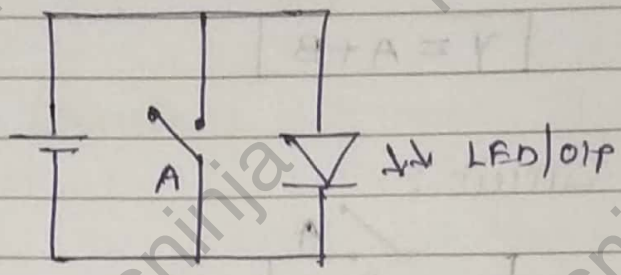
Defⁿ : It performs complement operation.

Logical Symbol :

Boolean Expression :

$$Y = \overline{A}$$

Switching Circuit :



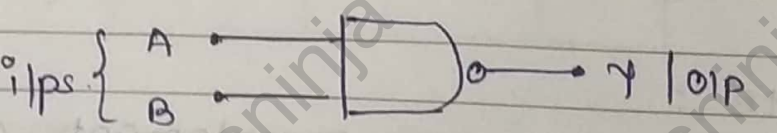
Truth Table :

Input	Output
A	$Y = \overline{A}$
0	1
1	0

4) NAND Gate :

Defⁿ : It is an universal gate because we can any Logic gates using this gate.

Logical Symbol :



Boolean Expression :

$$Y = \overline{A \cdot B}$$

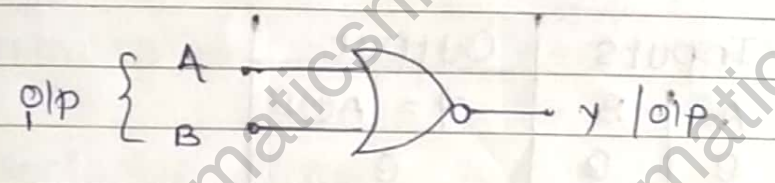
Truth Table :

Inputs		Output
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

5] NOR Gate :

Defn : It is an universal gate because we can construct any logic by using this gate.

Logical Symbol :



Boolean Expression :

$$\boxed{Y = \overline{A+B}}$$

Truth Table :

Inputs		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

6] Ex-OR Gate :

Defn : The o/p of Ex-OR gate is high for odd combination of inputs and low for even combination of inputs.

Logical Symbol :

Boolean Expression :

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

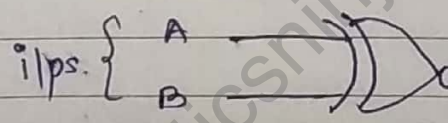
Truth Table :

Inputs		Output
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

7] Ex-NOR Gate :

Defn : The o/p of Ex-NOR gate is high if both the i/ps are even & low if both the i/ps are not identical.

Logical Symbol :



Boolean Expression :

$$Y = \overline{A \oplus B} = AB + \bar{A}\bar{B}$$

Truth Table :

I/ps		O/p
A	B	$Y = \overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

1.2 Boolean Algebra :

* Laws of Boolean algebra :

1) Commutative law : $A+B = B+A$

$A \cdot B = B \cdot A$

2) Associative law : $(A \cdot B) \cdot C = A \cdot (B \cdot C)$

$(A+B)+C = A+(B+C)$

3) Distributive law : $A \cdot (B+C) = AB + AC$

4) AND laws :

$A \cdot 0 = 0$

$A \cdot 1 = A$

$A \cdot A = A$

$A \cdot \overline{A} = 0$

5) OR laws :

$A+0 = A$

$A+1 = 1$

$A+A = A$

$A+\overline{A} = 1$

6) Inversion law :

$\overline{\overline{A}} = A$

7) Other laws :

$A \cdot BC = (A+B) \cdot (A+C)$

$\overline{A}+AB = \overline{A}+B$

$\overline{A}+A\overline{B} = \overline{A}+\overline{B}$

$A+AB = A+B$

$A+\overline{A}B = A+B$

* Duality Theorem :

"It states that, dual of an algebric expression can be obtained by replacing a binary 1 by a binary 0 and by interchanging the AND and OR operators"

e.g.

⇒ $A \cdot (B+C) = AB+AC$

dual is $A + (B \cdot C) = (A+B) \cdot (A+C)$

Q. Obtain the dual of following boolean eq^n.

1) $A + AB = A$

dual is $A \cdot (A+B) = A$

2) $A + \overline{A}B = A + B$

dual is $A \cdot (\overline{A} + B) = A \cdot B$

3) $A + \overline{A} = 1$

dual is $A \cdot \overline{A} = 0$

* De-Morgan's Theorem's:

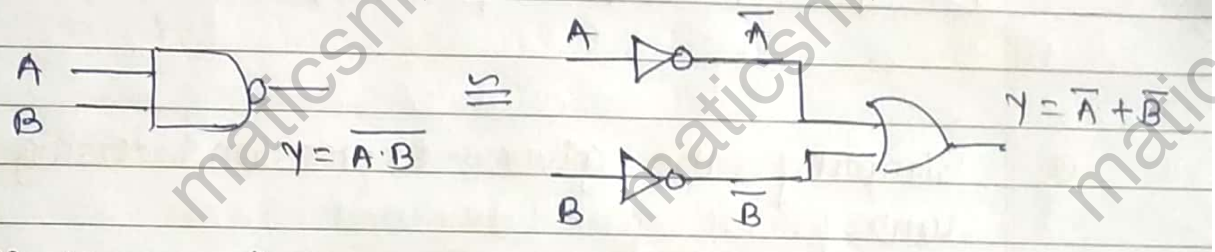
1) Theorem 1 :

Statement : This theorem states that the complement of product is equal to addition of the complements.

Logical Expression :

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

Logical Symbol :



Verification using Truth table :

A	B	$\overline{A}$	$\overline{B}$	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0

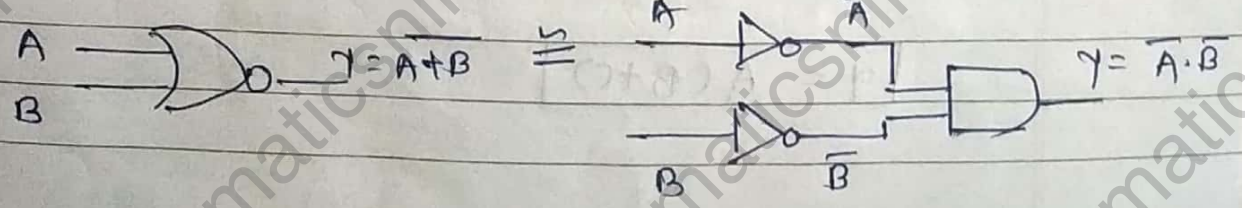
Theorem 2 :

Statement : This theorem states that the complement of sum is equal to product of complements.

Logical Expression :

$$\boxed{\overline{A+B} = \overline{A} \cdot \overline{B}}$$

Logical Symbol ;



Verification using truth table -

A	B	$\bar{A}$	$\bar{B}$	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1	1	1
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	0	0

Q Simplify the given expressions using boolean laws

1) $Y = (A+B)(A+C)$

→

$Y = AA + AC + BA + BC$

$Y = AA + AC + AB + BC$

$Y = A + AC + AB + BC$

$Y = A(1 + C + B) + BC$

$Y = A(1) + BC$

$\boxed{Y = A + BC}$

2) $Y = ABC + A\bar{B}C + AB\bar{C}$

→

$Y = ABC + A\bar{B}C + AB\bar{C}$

$Y = AC(B + \bar{B}) + AB\bar{C}$

$Y = AC(1) + AB\bar{C}$

$Y = AC + AB\bar{C}$

$Y = A(C + B\bar{C})$ $(\because B\bar{C} + C = C + B)$

$Y = A(C + B)$

$\boxed{Y = A(B + C)}$

3] $Y = AB + A\bar{B} + \bar{A}C + \bar{A}\bar{C}$

→ $Y = AB + A\bar{B} + \bar{A}C + \bar{A}\bar{C}$

$= A(B+\bar{B}) + \bar{A}(C+\bar{C})$

$= A(1) + \bar{A}(1)$

$= A + \bar{A}$

$= 1$

$\boxed{Y = 1}$

4) Prove that $(A+\bar{B}+AB)\cdot(A+B)\,\bar{A}\cdot\bar{B} = 0$

→ LHS $= (A+\bar{B}+AB)\cdot(A+B)\cdot\bar{A}\cdot\bar{B}$

$= (A+\bar{B}+AB)(A\cdot\bar{A}\cdot\bar{B} + B\cdot\bar{A}\bar{B})$

$= (A+\bar{B}+AB)\cdot 0$

$= 0$

$=$ RHS

1.3 Logic families :

Characteristics of logic families :-

1) Noise Margin :
The amount of extraneous signal which can be tolerated before an output voltage of gate deviated from allowed logic voltage level.

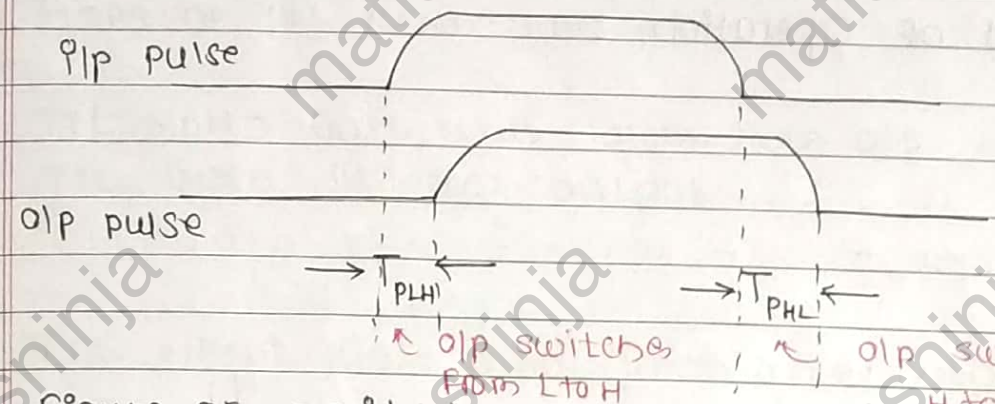
2) Power dissipation :
The amount of power dissipated at the o/p in the form of heat resulting in increase in temperature is called as power dissipation.

$$P_{D(avg)} = \frac{P_{DH} + P_{DL}}{2}$$

P_{DH} = Power dissipated when i/p was high
P_{DL} = Power dissipated when i/p was low

3] Propagation delay :

The time taken by particular gate to produce o/p when i/p is applied is called as propagation delay.



4] figure of merit :

The product of propogation time and power dissipation is known as figure of merit.

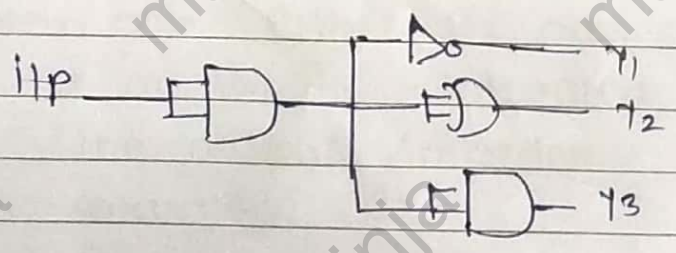
5] fan in :

Number of inputs connected to gate is called as fan in of the gate.

e.g. 2 input NAND gate has fan in = 2

6] fan out :

Number of load gates connected at the output of gate is called fanout of the gate



Above circuit has fan out = 3

Speed of Operation :

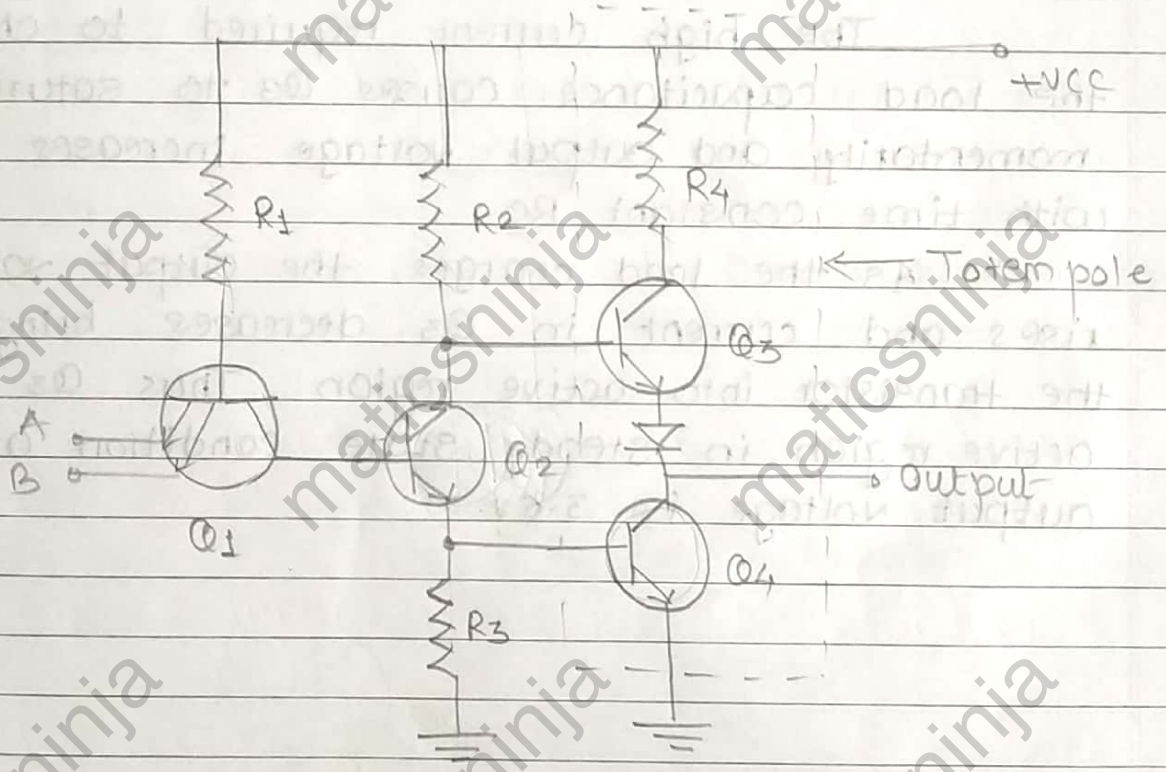
* Comparision of TTL, CMOS & ECL.

	Parameter	TTL	CMOS	ECL
1)	Basic Gates	NAND	NOT	OR-NOR
2)	Fan-out	10	50	25
3)	Propagation delay	10ns	70-105 ns	2 ns
4)	Power dissipation	10 mW	1.01 mW	40-55 mW
5)	Speed power product	100 PJ	0.7 PJ	100 PJ
6)	clock rate	35 MHz	10 MHz	760 MHz

* Types of TTL NAND gate :

1) TTL NAND Gate with Totem-pole o/p.
2) TTL open collector output.

1) TTL NAND Gate with Totem pole output :



Totem pole transistors are used because they produce a low output. Transistors Q3 and Q4 form a totem pole. Either Q3 acts as an emitter follower or Q4 is saturated.

The output impedance is low even when Q4 is saturated.

The output impedance of gate is not purely resistive but is partially capacitive.

The totem pole output reduces propagation delay considerably.

When o/p is low, Q_2 and Q_4 are in saturation. Diode D_1 is provided to ensure that Q_3 is cut-off when Q_4 is saturated. As the output changes to a high state the transistors Q_2 & Q_4 go into cut-off region. As soon as Q_2 turns off, Q_3 starts conducting because the base of Q_3 is connected to V_{cc}.

The high current required to charge the load capacitance causes Q_3 to saturate momentarily and output voltage increases with time constant RC.

As the load charges, the output voltage rises and current in Q_3 decreases, bringing the transistor into active region. Thus Q_3 in active region in steady state condition and output voltage is 3.6 V.

TTL Open Collector Output :

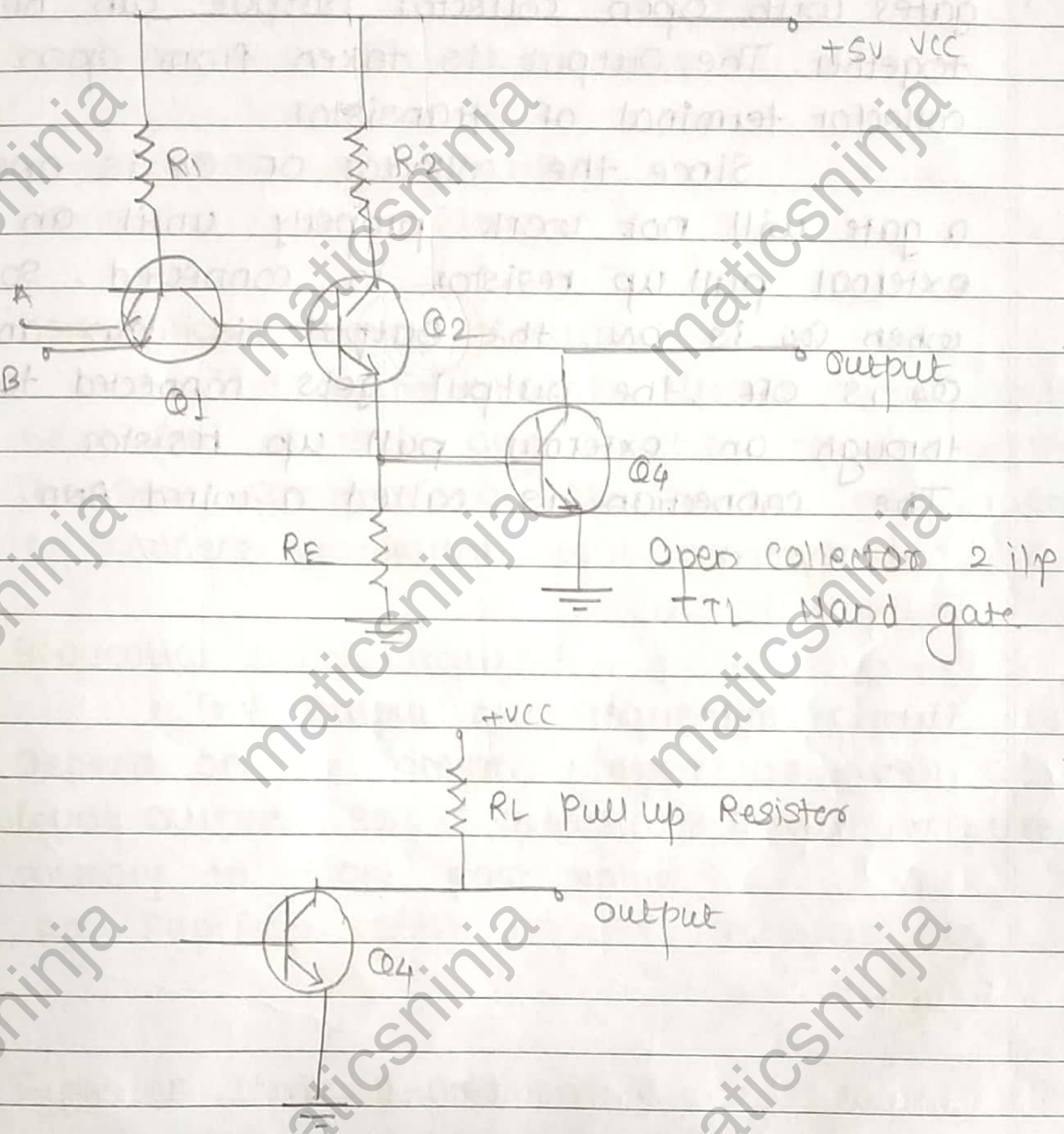


fig Open collector output with pull up resistor

The totem pole output has a drawback that two outputs cannot be tied together. If the totem pole outputs of two separate gates are tied together then a high current may cause overheating and deteriorate the

performance, resulting in a device failure.

Some TTL devices provides an open collector output. The outputs of two different gates with open collector output can be tied together. The output is taken from open collector terminal of transistor.

Since the collector of Q_4 is open, a gate will not work properly until an external pull up resistor is connected, so that when Q_4 is ON, the output is low and Q_4 is OFF, the output gets connected to V_{cc} through an external pull up resistor.

The connection is called a wired AND.