Practical No.6: Implement 2 input, 3 input Adder Circuit.

I Practical Significance

In many computers and other kinds of processors, adders are used in the arithmetic logic units (ALUs). They are also used in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators and similar operations.

II Industry/Employer Expected Outcome(s)

Students will be able to test the functionality of the digital circuits/system.

III Course Level Learning Outcome(s)

Develop combinational logic circuits for given applications.

IV Laboratory Learning Outcome(s):

1. Verify the truth table of Half and Full adder circuits for the given input.

V Relevant Affective Domain related outcome(s)

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

VI Relevant Theoretical Background

A half adder is a digital logic circuit that performs binary addition of two single-bit binary numbers. It has two inputs, A and B, and two outputs, SUM(S) and CARRY (C). The SUM output is the least significant bit (LSB) of the result, while the CARRY output is the most significant bit (MSB) of the result, indicating whether there was a carry-over from the addition of the two inputs. The half adder can be implemented using one EX-OR gate and one AND gate. The C output is 1 only when both inputs are 1.

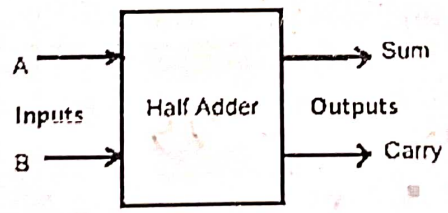


Fig 6.1:Block Diagram of Half adder

The full adder is a combinational circuit which is used to perform addition of three input bits. The full adder adds the bits A and B and the carry from the previous bits addition called the carry in (Cin) and the outputs the sum bit (S) and the carry bit called the carry out (Cout). The variable S gives the value of the least significant bit of the sum. The variable Cout gives the output carry.

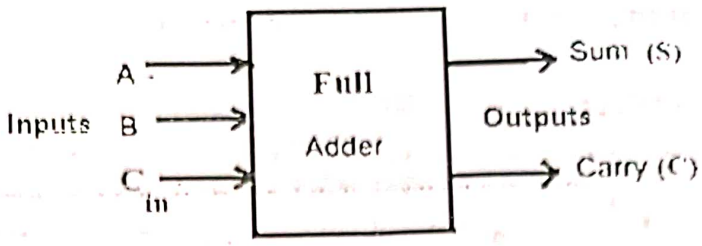


Fig 6.2: Block Diagram of Full adder

VII Circuit diagram

a) Sample circuit

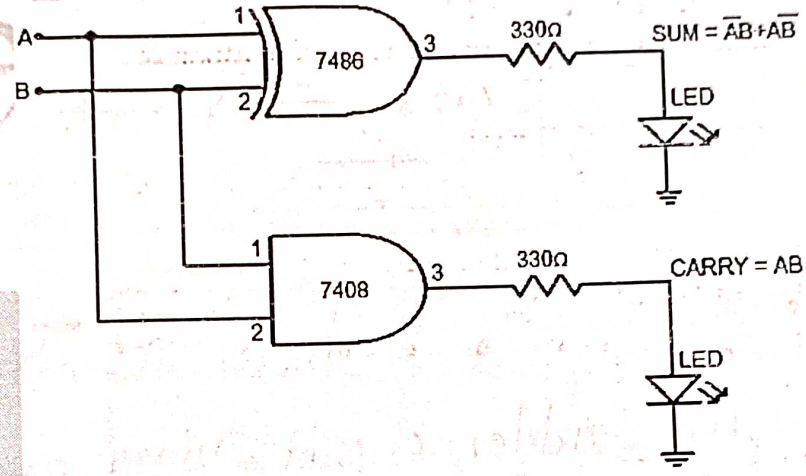


Fig 6.3: Half adder Circuit Diagram

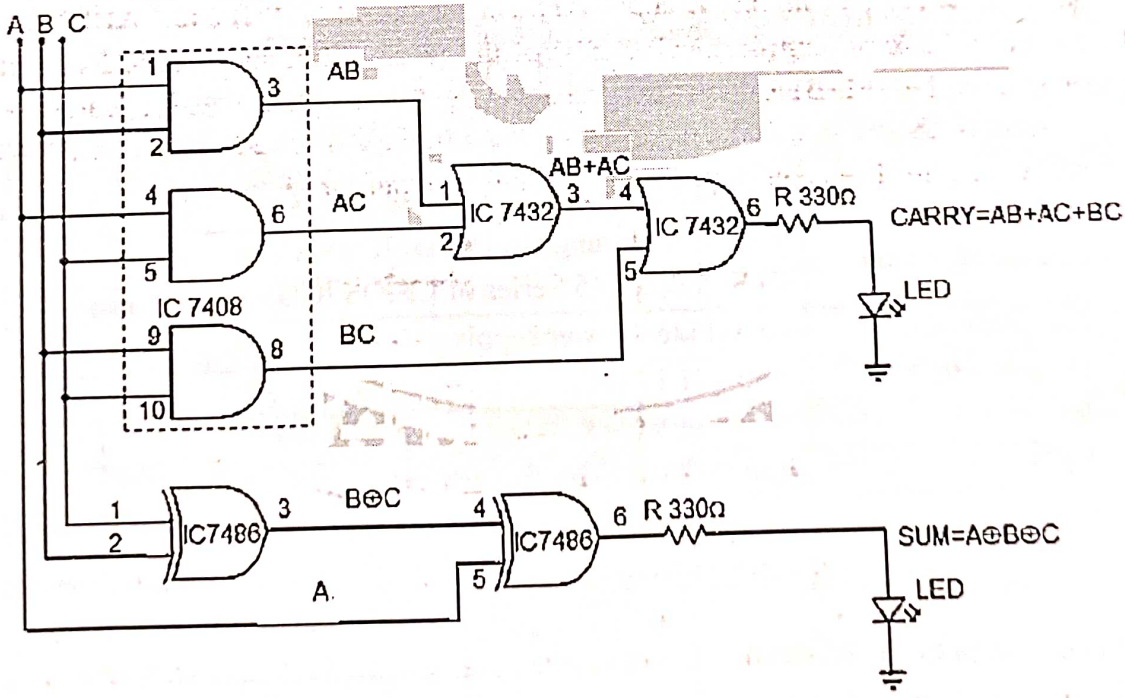
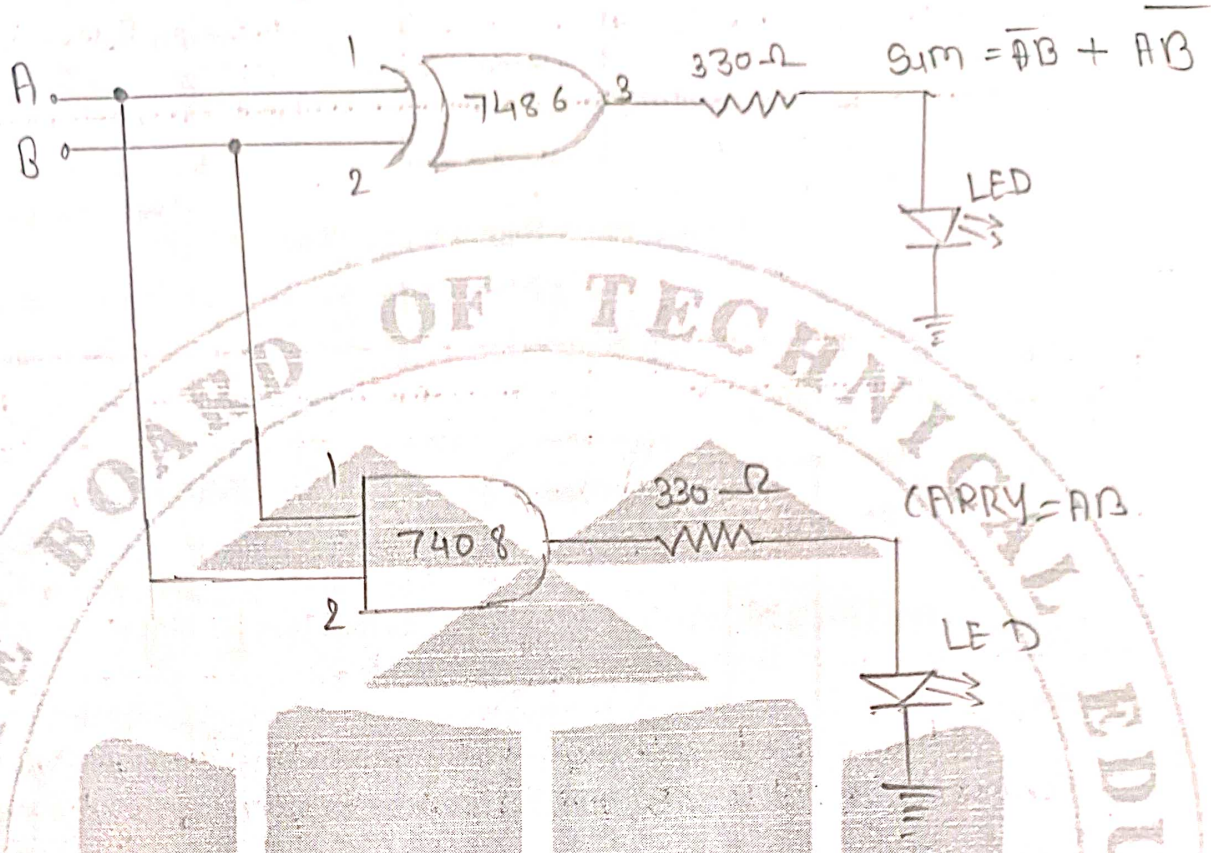


Fig 6.4: Full adder Circuit Diagram

b) **Actual circuit**



Half adder circuit Diagram

VIII Resources Required

Sr. No.	Name of Resource	Suggested Broad Specification	Quantity
1	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1
3	DC power supply	+5 V Fixed power supply	1
4	Breadboard	5.5cm X 17 cm	1
5	IC	7486, 7408,7432.	1 Each
6	LED	Red /Yellow color 5 mm	1
7	Connecting wires	Single strand 0.6 mm Teflon coating	As required
8	Resistor	1KΩ/330Ω	As required

IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

X Procedure

1. Test the IC using Digital IC tester
2. Mount the IC on the breadboard and Make the connection as per figure 6.3.
3. Connect the +5V to +Vcc pin of IC and GND pin to ground
4. Observe the LED (on or off) for each combination of input as per truth table
5. Verify the truth table
6. Repeat the procedure for figure 6.4.

XI Resources Used

Sr. No.	Name of Resource	Suggested Broad Specification	Quantity
1	Digital multimeter	3½ digit display	2
2	Breadboard	5.5cm × 17cm	1
3	IC	7486, 7408, 7432	1 each
4	Resistor	1kΩ / 330Ω	as required

XII Actual Procedure

1. Test the IC using digited IC tester
2. Connect the +5V to +Vcc pin of IC and GND pin to ground
3. Verify the truth table
4. Repeat the procedure for fig 6.4

XIII Observation:

Table 6.1: Observation Table for Half Adder

Inputs		Output			
		Sum		Carry	
A	B	Logic Level (1/0)	Output voltage (v)	Logic Level (1/0)	Output voltage (v)
0 (0V)	0(0V)	0	0V	0	0V
0(0V)	1(5V)	1	4.5V	0	0V
1(5V)	0(0V)	1	4.5V	0	0V
1(5V)	1(5V)	0	0V	1	4.5V

Table 6.2: Observation Table for Full Adder

Inputs			Output			
			Sum		Carry	
A	B	C	Logic Level (1/0)	Output voltage (v)	Logic Level (1/0)	Output voltage (v)
0 (0V)	0(0V)	0(0V)	0	0V	0	0V
0(0V)	0(0V)	1(5V)	1	4.5V	0	0V
0(0V)	1(5V)	0(0V)	1	4.5V	0	0V
0(0V)	1(5V)	1(5V)	0	0V	1	4.5V
1(5V)	0(0V)	0(0V)	1	4.5V	0	0V
1(5V)	0(0V)	1(5V)	0	0V	1	4.5V
1(5V)	1(5V)	0(0V)	0	0V	1	4.5V
1(5V)	1(5V)	1(5V)	1	4.5V	1	4.5V

XIV Result(s)

In this Practical we learn about how to implement 2 input & 3 input Adder circuit.

XV Interpretation of results

In this practical we observe the implementation of 2 input and 3 input adder circuit.

XVI Conclusion and recommendation

Hence, we learnt how to implement 2 input and 3 input adder circuit.

XVII Practical related questions

Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

1. State drawback of Half Adder circuit.
2. Draw half adder using NAND gates only.
3. Design Half Adder using K-map.
4. Draw Full adder circuit using Half adder circuits.

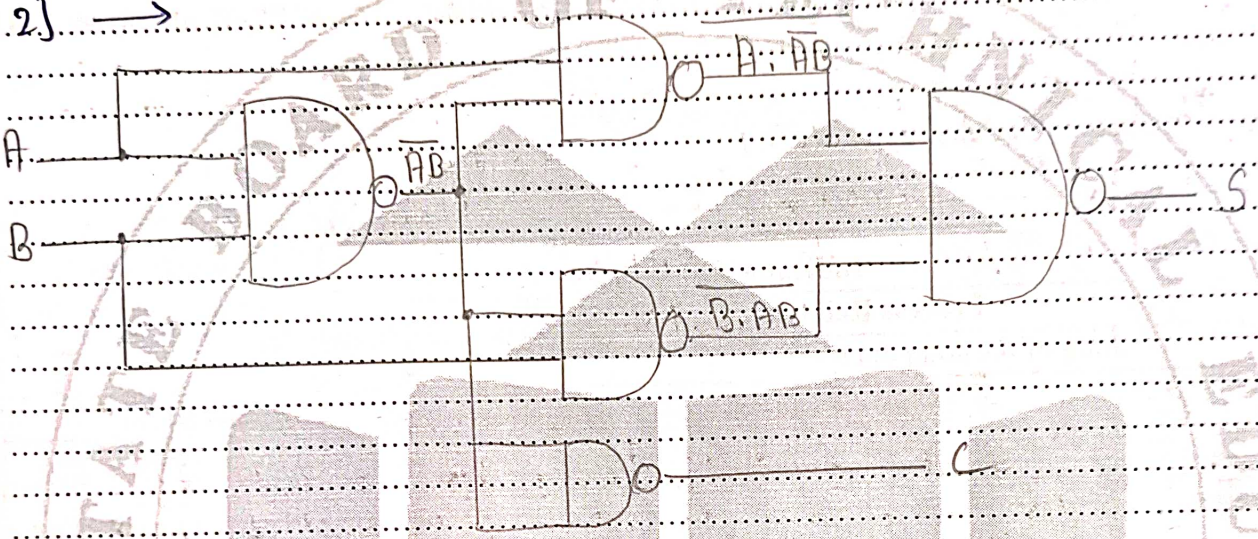
[Space for Answers]

1] →

Here are some specific limitations

1. No carry input
2. No carry output
3. Limited bit width
4. Incomplete representation

2] →



3] →

K-map For Sum

A\B	0	1
0	1	1
1	1	

$Sum = A'B + AB'$

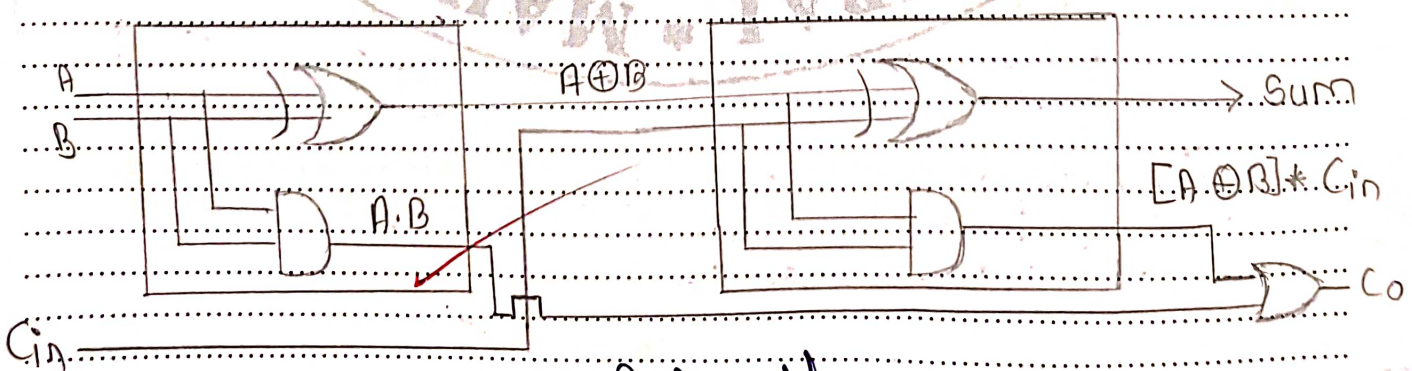
K-map For Carry

A\B	0	1
0		
1		1

$Carry = AB$

4] →

Half Adder -1 Half Adder -2



full adder

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XVIII References/Suggestions for further reading

1. https://de-iitr.vlabs.ac.in/exp/half-full-adder/index.html
2. https://www.futurlec.com/74/IC7402.shtml
3. https://www.ntchip.com/electronics-news/ic-7486-chip
4. https://www.ti.com/lit/ds/symlink/sn5432.pdf?ts=1720330546912&ref_url=https%253A%252F%252Fwww.google.com%252F

XIX Assessment Scheme

	Performance Indicators	Weightage
	Process Related : 15 Marks	60 %
1	Handling of the components	10%
2	identification of components	20%
3	Measuring value using suitable instrument	20%
4	working in teams	10%
	Product Related: 10 Marks	**40%**
5	Calculated theoretical values of given component	10%
6	Interpretation of result	05%
7	Conclusion	05%
8	Practical related questions	15%
9	Submitting the journal in time	05%
	Total (25 Marks)	**100 %**

Marks Obtained			Dated signature of Teacher
Process related (15)	Product related (10)	Total (25)	
13	10	23	