Practical No.12: Implement and verify the truth table of RS Flip-flop.

I Practical Significance

A Flip-Flop is a basic digital logic circuit use for storing binary information. It is also known as One bit memory. It has two stable states typically 0 (reset) and 1 (set), and it can maintain its current state until it is instructed to change it by applying a clock pulse. Flip-Flops are fundamental building blocks in digital electronics, used in memory storage, sequential logic circuits and Data synchronization.

II Industry/Employer Expected Outcome(s)

Students will be able to test the functionality of the digital circuits/system.

III Course Level Learning Outcome(s)

Develop sequential logic circuits using Flip-Flops.

IV Laboratory Learning Outcome(s):

1. Build/Test functionality of RS flip flop using NAND Gate.

V Relevant Affective Domain related outcome(s)

Flip-Flop data holding/storing ability.
Handle the component and equipment carefully.
Follow all safety precaution

VI Relevant Theoretical Background

Digital circuits have many combinations of logic circuits. They are classified as either combinational or sequential. The output of combinational circuits depends only on the current inputs. In contrast, sequential circuit depends not only on the current value of the input but also upon the internal state of the circuit. Basic building blocks (memory elements) of a sequential circuit are the flip-flops (FFs). The FFs change their output state depending upon inputs at certain interval of time synchronized with some clock pulse applied to it.

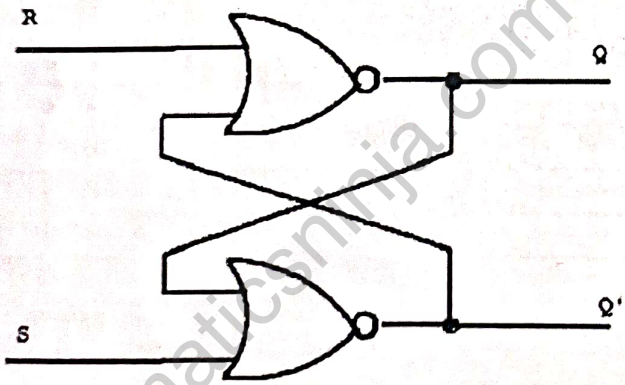
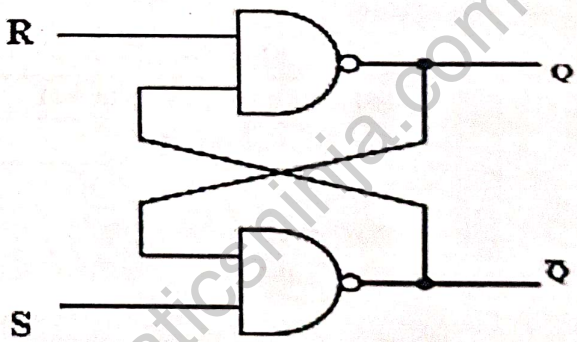


Fig 12.1 a) SR latch using NOR gates



b) SR latch using NAND gates

S	R	Q	$\overline{Q}$
0	0	Same as previous	Same as previous
0	1	0	1
1	0	1	0
1	1	Race	Race

S	R	Q	$\overline{Q}$
0	0	Race	Race
0	1	0	1
1	0	1	0
1	1	Same as previous	Same as previous

Fig 12.2 Truth table for Circuit diagram in Fig 12.1 a&b

VII Circuit diagram

a) Sample circuit

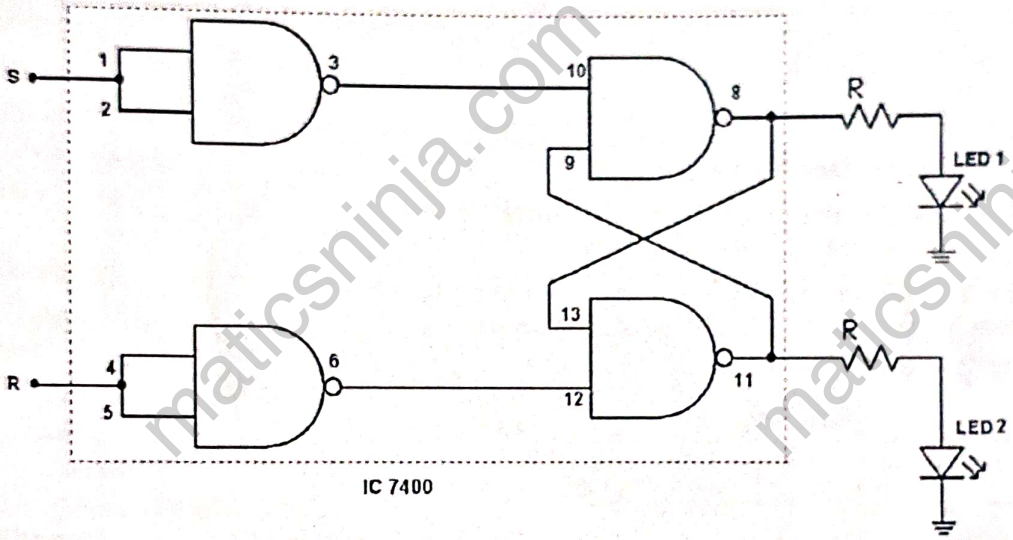
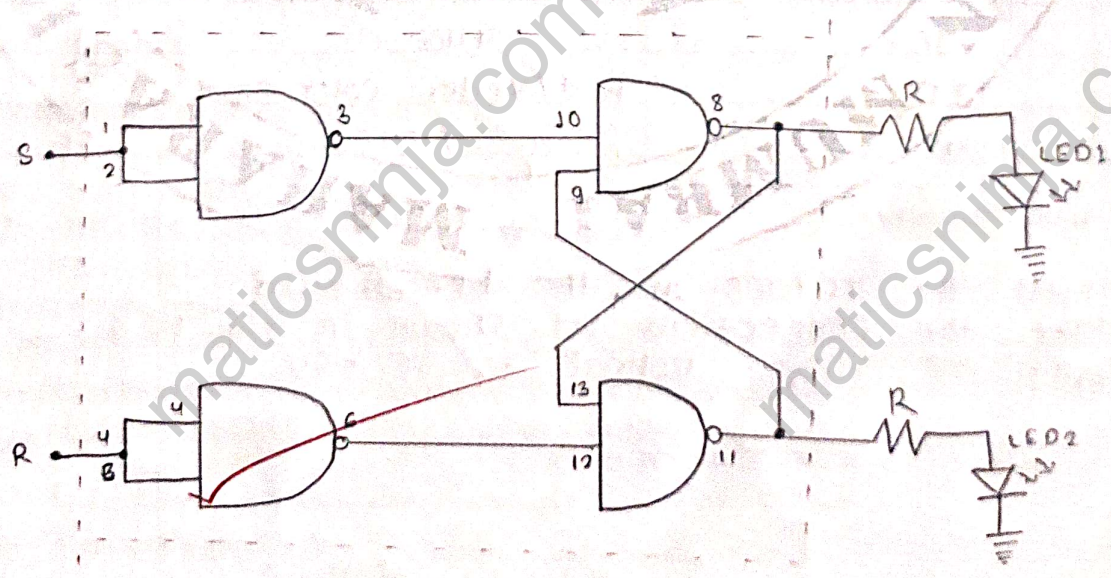


Fig 12.3 SR Flip-Flop using NAND gates

b) Actual circuit



VIII **Resources Required**

Sr. No.	Name of Resource	Suggested Broad Specification	Quantity
1	Digital Multimeter	3 ½ digit display	1 or 2
2	Digital IC Tester	Tests a wide range of digital IC's such as 74 series, 40/45 series of CMOS IC's	1
3	DC Power supply	+5 V fixed power supply or Variable DC power supply (0-30V)	1
4	Breadboard	5.5cm X 17cm	1
5	Connecting Wires	Single strand wires of 0.6 mm	As per Requirement
6	IC	7400	1
7	LED	Red/Yellow color 5 mm	2
8	Resistor	220Ω/330Ω	4

IX **Precautions to be followed**

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

X **Procedure**

1. Mount the IC7400 on the breadboard.
2. Make the connections as shown in figure 12.3
3. Apply the supply voltage to IC +5V.
4. Apply inputs according to the observation table.
5. Observe the LED (on or off) for each combination of input as per truth table.
6. Verify the truth table.

XI **Resources Used**

Sr. No.	Name of Resource	Suggested Broad Specification	Quantity
1>	Breadboard	5.5cm X 17cm	1
2>	IC	7400	1
3>	LED	Red/Yellow Color 5mm	2
4>	resistor	220Ω / 330Ω	4

XII **Actual Procedure**

1> Mount the IC7400 on the breadboard
2> Make the connections as shown in fig. 12.3
3> Apply the supply voltage to IC +5V

4) Apply inputs according to the observation table
5) Observe the LED (on or off) for each combination on input as per truth table
6) Verify the truth table

XIII Observation:

Table 12.1: Observation Table for SR Flip-Flop

Inputs		Q		$\bar{Q}$		Remark
S	R	Logic Level (0/1)	Output Voltage (V)	Logic Level (0/1)	Output Voltage (V)	
0 (0V)	0 (0V)	no change	depend on previous	compliment of previous	depend on previous	no change
1 (5V)	0 (0V)	1	5V	0	0V	set
0 (0V)	1 (5V)	0	0V	1	5V	reset
1 (5V)	1 (5V)	undefined	undefined	undefined	undefined	undefined

XIV Result(s)

In this practical we studied implement & verify the truth table of RS flip-floop.

XV Interpretation of results

In this practical we studied to implement & verify the truth table of RS flip-floop.

XVI Conclusion and recommendation

Hence we studied to implement & verify the truth table of RS flip-floop.

XVII Practical related questions

Note: Below given are few sample questions for reference. Teacher must design more suchquestions so as to ensure the achievement of identifies CO.

1. Why the Name of Flip-Flop is given SR Flip-Flop?
2. Explain the Race Condition in SR Flip-Flop?
3. List how race condition can be resolved?
4. State application of SR Flip-Flop?

Q.1) ⟶

The term "SR flip-flop" derives from its two primary inputs : S (set) & R (Reset).

1) S(set) :

This input sets the output of the flip-flop to a high state (1) when the set input is activated the flip-flop output a high signal.

2) R(Reset) :

This input is activated (R=1 & S=0) it resets the output Q to 0, there by storing a logic low state.

Q.2) ⟶

A race condition in an SR flip-flop occurs when both the set (S) & Reset (R) input are activated simultaneously or in rapid succession, creating an ambiguous state.

Q.3) ⟶

problem with race condition can be solved by adding an assurance that no other process can accessed the shared resource while a process is using it reads or write the period of time for the assurance it called the crucial section.

Q.4) ⟶

memory stroage :

The SR flip-flop is used in memory storage devices such as registar which are used to store data temporary registers are used in a oride range of applications including microprocessors, digital signals processor & other digital circuit.

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XVIII References/Suggestions for further reading

1. https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/ (Virtual Lab Link on SR Flip-Flop)
2. https://www.youtube.com/watch?v=jm0PGDSSBkI (NPTEL Video Link on Latch and Flip-Flop (Part 1))
3. https://www.youtube.com/watch?v=i-tnQMDdbfc (NPTEL Video Link on Latch and Flip-Flop (Part 2))

XIX Assessment Scheme

	Performance Indicators	Weightage
	Process Related : 15 Marks	**60 %**
1	Handling of the components	10%
2	identification of components	20%
3	Measuring value using suitable instrument	20%
4	working in teams	10%
	Product Related: 10 Marks	**40%**
5	Calculated theoretical values of given component	10%
6	Interpretation of result	05%
7	Conclusion	05%
8	Practical related questions	15%
9	Submitting the journal in time	05%
	Total (25 Marks)	**100 %**

Marks Obtained			Dated signature of Teacher
Process related (15)	Product related (10)	Total (25)	
12	10	22	